Abstract of the disclosure

A non-volatile memory device includes a cell region and a peripheral circuit region at the semiconductor substrate. A plurality active regions are disposed in the cell region in parallel with each other. A plurality of cell line patterns cross over the active regions in parallel. A couple of tunnel insulating layers and the floating gate electrodes are disposed between the cell line patterns and the active regions. A dummy region is interposed between the cell region and the peripheral circuit region where at least one dummy line pattern is disposed in the dummy region.